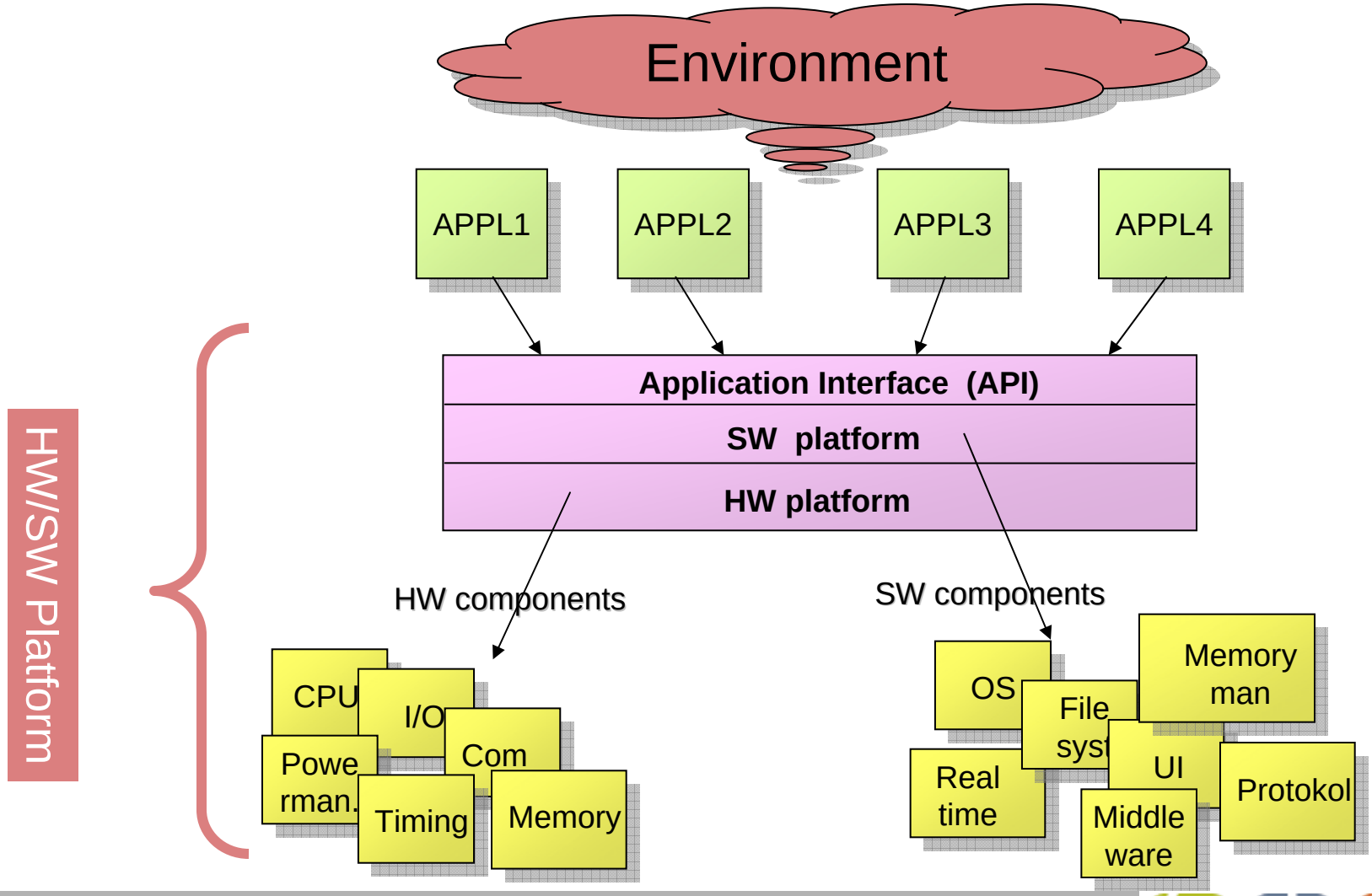
Challenges from my perspective

UPPAAL over den Embeddede Verden

Kim Guldstrand Larsen

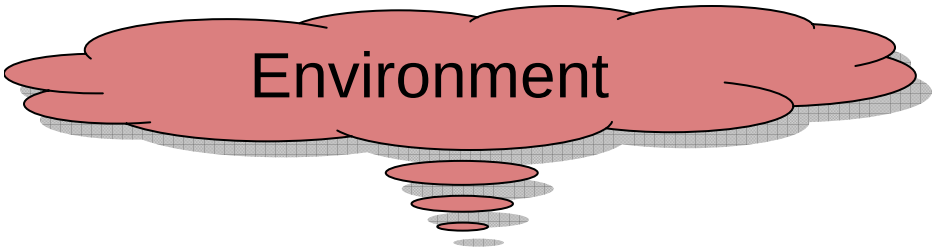
Center for Embedded Systems
Department of Computer Science
Aalborg University
DENMARK

Embedded Systems – Levels



Embedded Systems – Formalisms

Ingeniøren ELEKTRONIK-08



$$u(t) = K_p e(t) + K_i \int^t + K_d \frac{de}{dt}$$

CONTROL THEORY

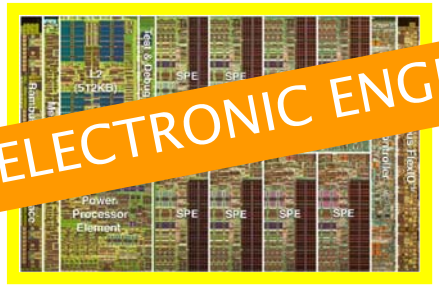
```
private void handleBrick() {
Sensors.synchronizedReadSensors();
int input = (Sensors.getBufferedSensor(0) + Sensors
                    .getBufferedSensor(1)) >> 1;

if (awaitingBrick) {
                    if (input > lastRead) {
                                        lastRead = input;
                    } else if ((lastRead - input) >= TRESHOLD) {
                                        awaitingBrick = false;
                                        if (lastRead > BRICK
                    brickFound(l
                    }
```

COMPUTER SCIENCE

APPL

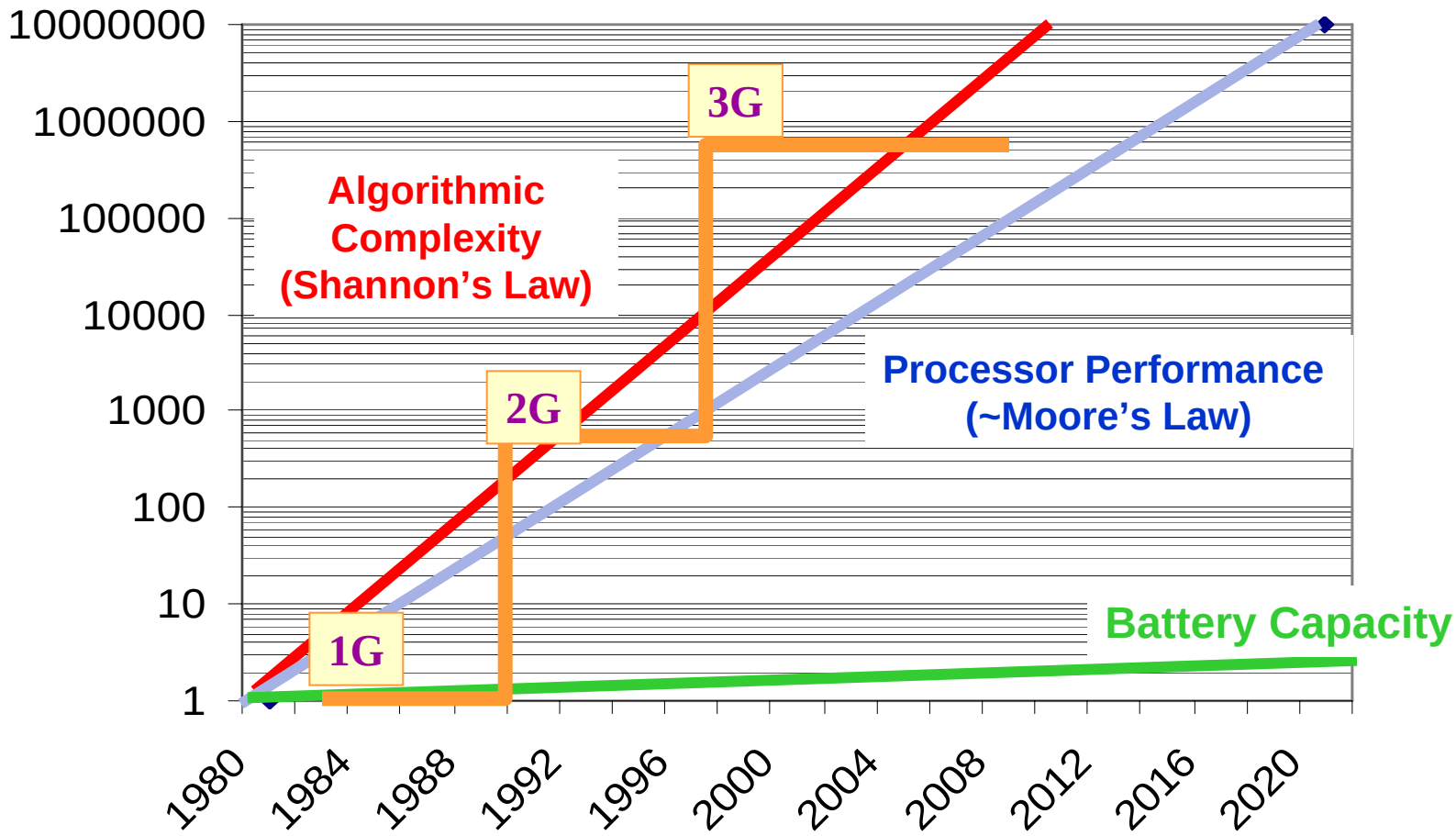
CPU
I/O
Powe
rman.
Kom
Timing
Memory



ELECTRONIC ENGINEERING

Technology Gaps

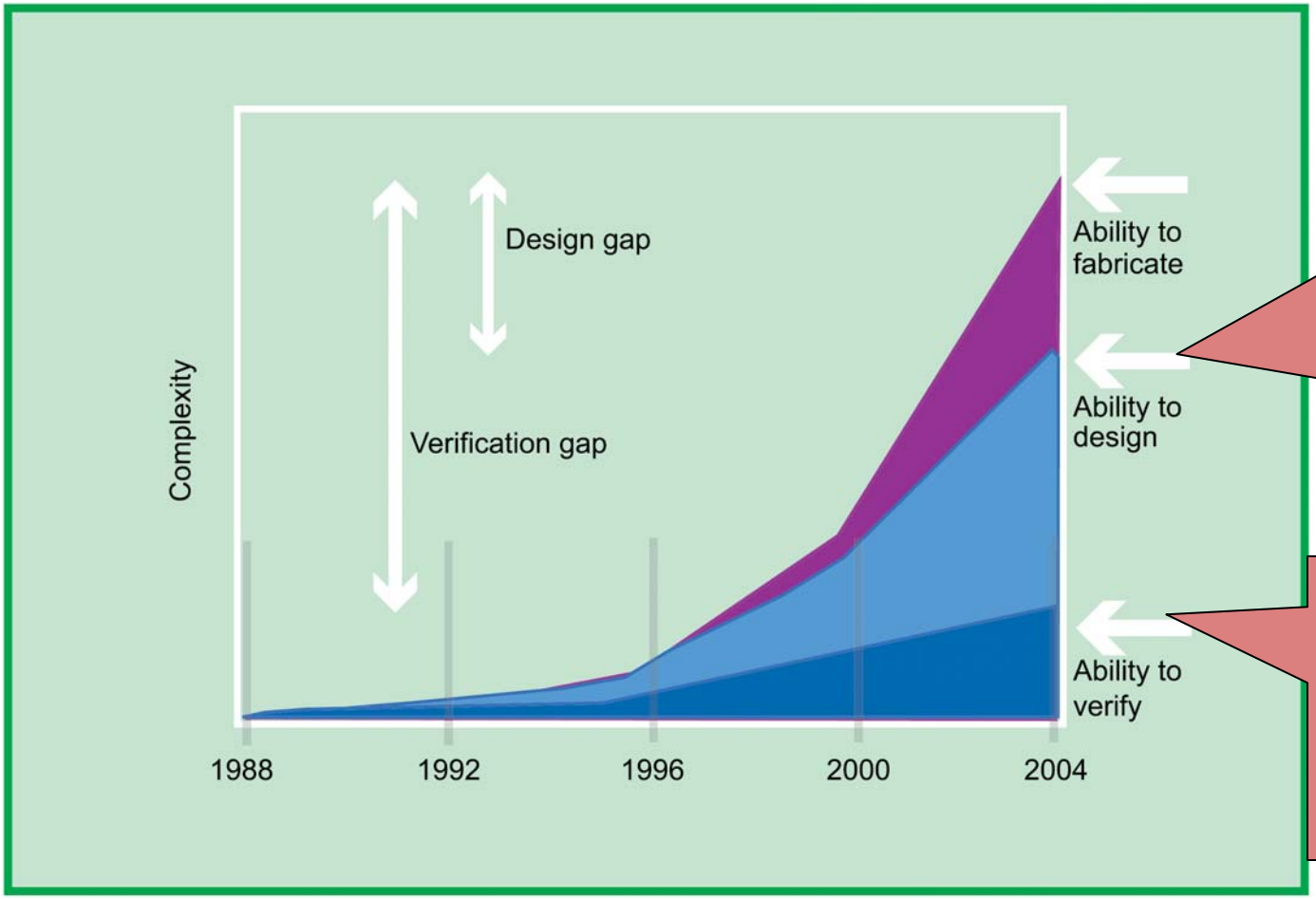
Ingeniøren ELEKTRONIK-08



Source: Data compiled from multiple sources (BWRC)

Design & Verification Gap

Ingeniøren ELEKTRONIK-08



Higher level programming languages (e.g. OO)
--
Component-based Dev.

Model-based Dev.
--
Simple platform

Brian Bailey, Chief Technologist, Design Verification and Test Division, Mentor Graphics Corp.

Java Object – Regional IKT Korridor

Ingeniøren ELEKTRONIK-08

- Productivity of a programmer is increased with up to 700 % by changing from C/C++ to Java !
- Number of well-educated Java programmers increasing !

- Java for hard real-time systems ?
- Java and C/Assembler legacy code ?

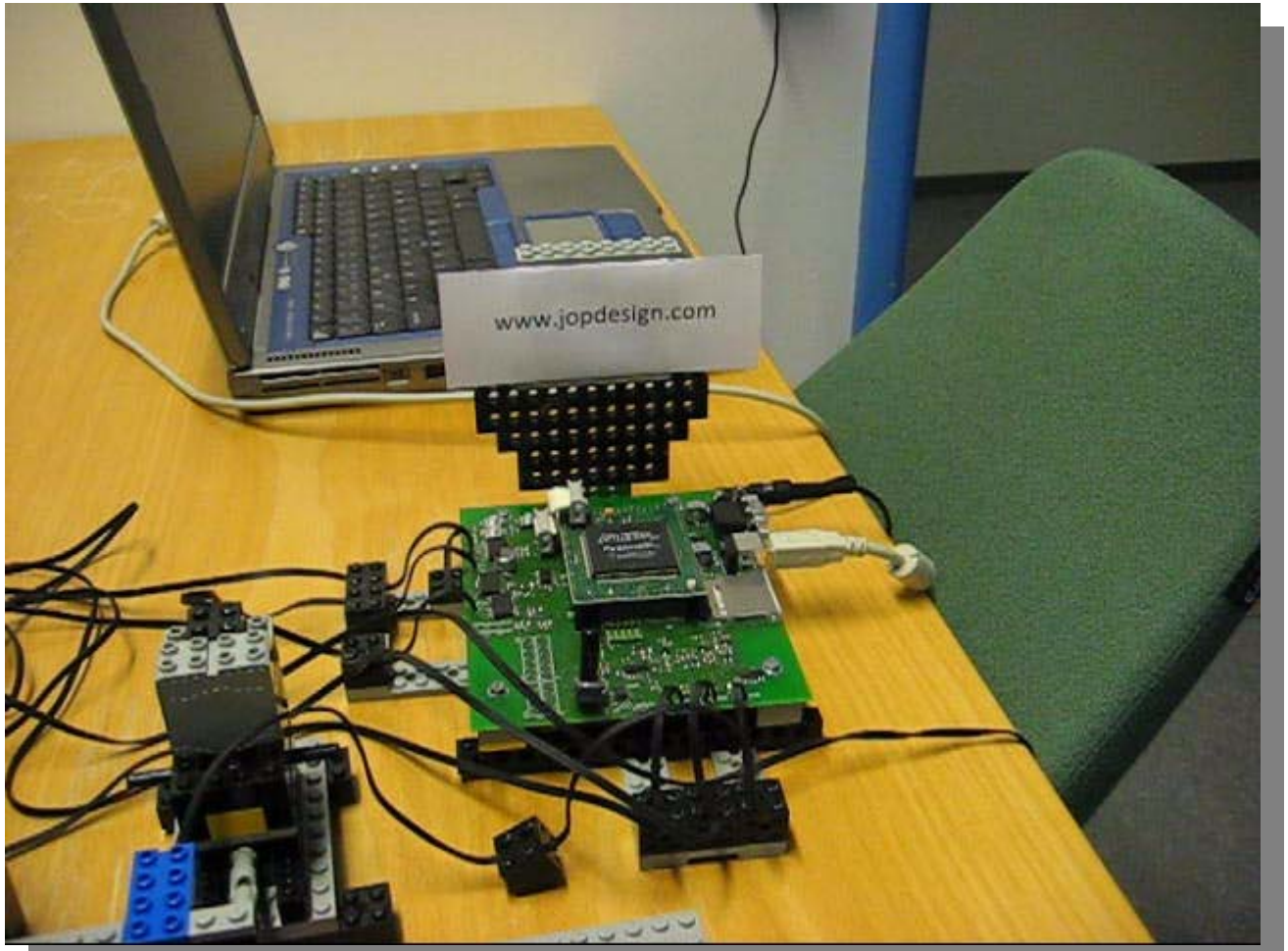
- Emerging new profiles and hardware implementations !
- Eclipse framework !

- Center for Embedded Software Systems
- Vitus Bering Denmark
- Polycom (Kirk Telecom A/S)
- Wirtek A/S
- Mechatronic Brick ApS
- Aalborg Industries A/S
- Prevas A/S
- Teknologisk Institut

- Tekkva Consult (project coordinator).

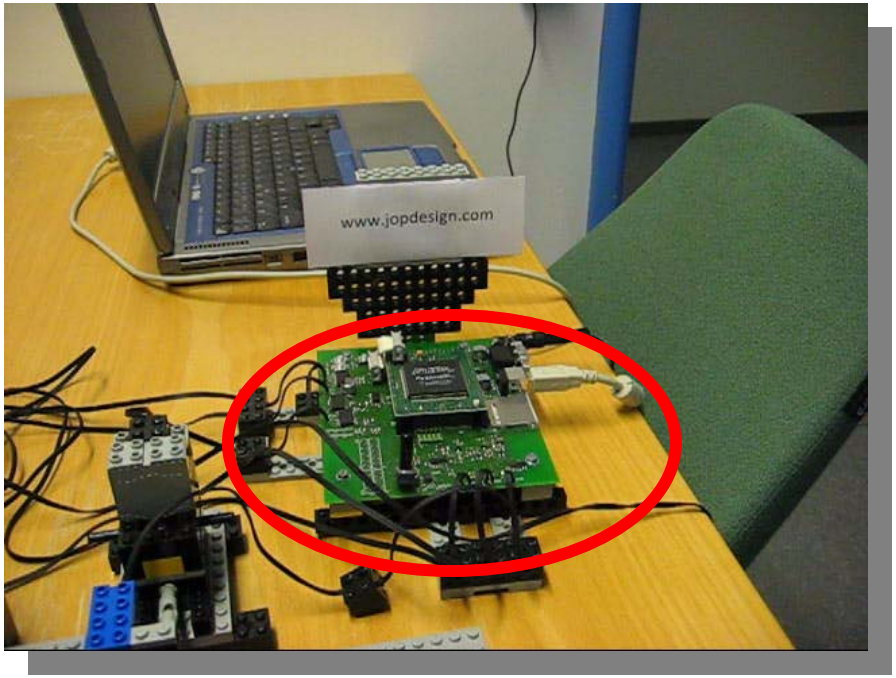
Real-Time Sorting

Ingeniøren
ELEKTRONIK-08



Hardware

Ingeniøren ELEKTRONIK-08



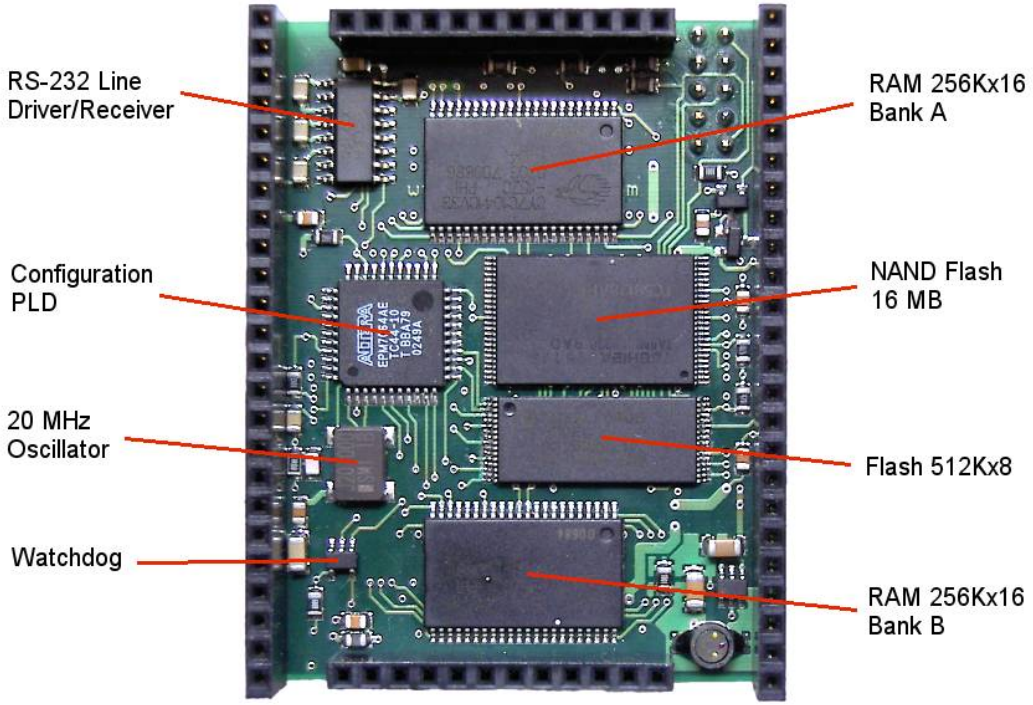
- JOP (Java Optimized Processor)
- Native execution of Java Bytecode
- Bytecode implemented in Microcode
- Avoid unpredictable data-cache
- Time predictable
- Developed new method and stack cache
- Implemented in FPGA

Java Optimizing Processor

Ingeniøren ELEKTRONIK-08

Martin Schöberl
University of Tech., Vienna

FPGA

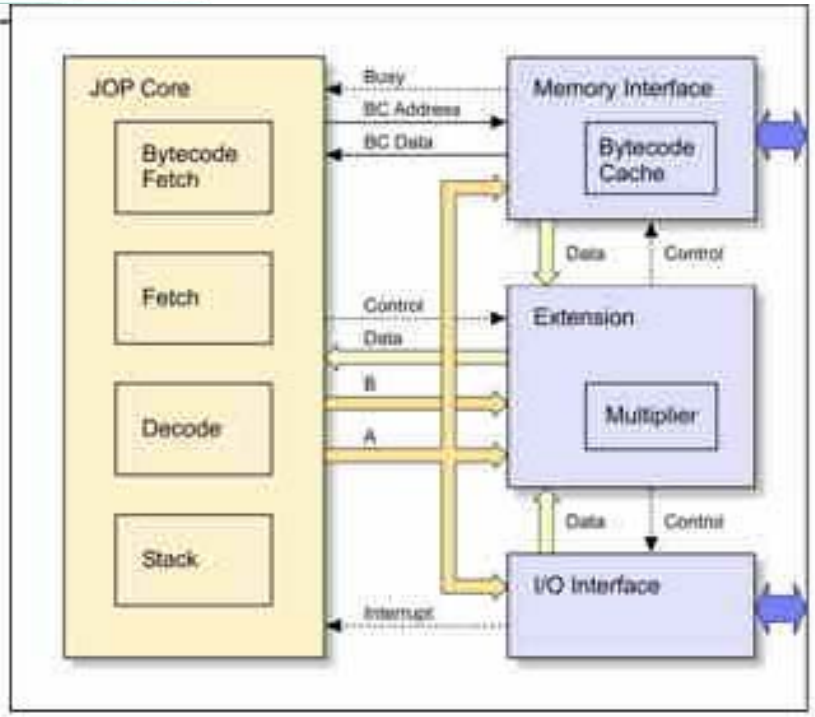


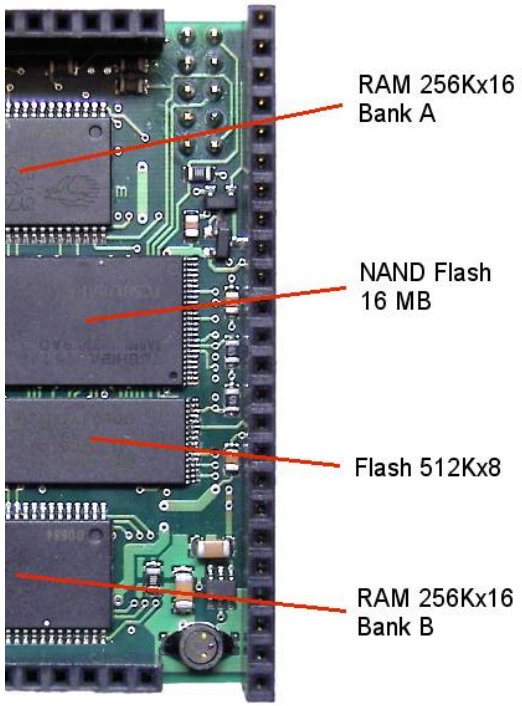
JOP Block Diagram

Ingeniøren ELEKTRONIK-08

FPGA

3-4 different FPGAs
6 different boards





Safety Critical Java

Ingeniøren ELEKTRONIK-08

Min interarrival

Tasks

Deadline

```
public static void main(String[] args) {
   new SporadicPushMotor(
        new SporadicParameters(4, 4000, 60), 0);
   new SporadicPushMotor(
        new SporadicParameters(2, 4000, 60), 1);

   PeriodicMotorSpooler motorSpooler =
        new PeriodicMotorSpooler(
              new PeriodicParameters(4000));

   new PeriodicReadSensor(
        new PeriodicParameters(2000), motorSpooler);

   RealtimeSystem.start();
}
```

Byte code – Micro code

Ingeniøren ELEKTRONIK-08

```
protected boolean run()
    if i<5 {
          i = i + 4;
    } else {
          i = i * 4;
    }
    return true;
}
```

```
Method: run ()Z
 0: aload_0
 1: getfield
 4: ifeq -> 20
 7: aload_0
 8: dup
 9: getfield
 12: iconst_1
 13: iadd
 14: putfield
 17: goto -> 30
 20: aload_0
 21: dup
 22: getfield
 25: iconst_1
 26: isub
 27: putfield
 30: iconst_1
 31: ireturn
```

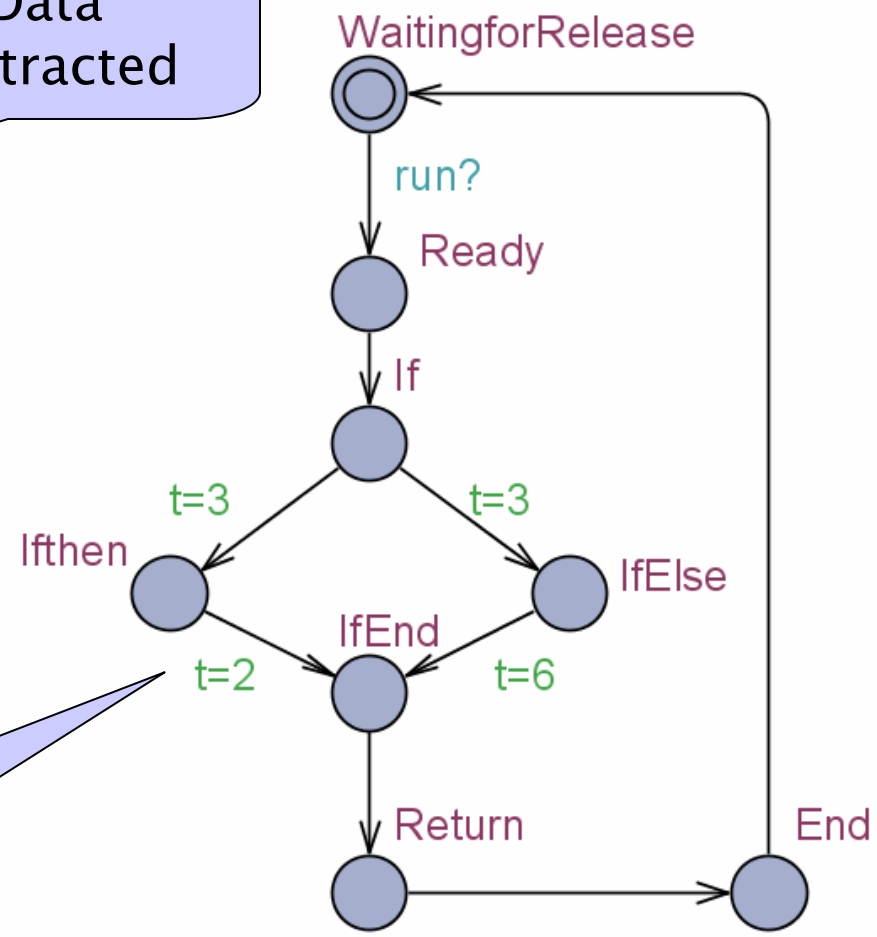
Byte code – Timed Automata

Ingeniøren ELEKTRONIK-08

```
protected boolean run()
    if i<5 {
        i = i + 4;
    } else {
        i = i * 4;
    }
    return true;
}
```

Data abstracted

Timing = WCET from microcode



SARTS – from Safety Critical Java

Ingeniøren ELEKTRONIK-08

```
public static void main(String[] args) {
        new SporadicPushMotor(
                new SporadicParameters(4, 4000, 60), 0);
        new SporadicPushMotor(
                new SporadicPa

        PeriodicMotorSpooler mo
                new PeriodicM
                        new

        new PeriodicReadSensor(
                new PeriodicPa

        RealtimeSystem.start();
}
```

TASKS

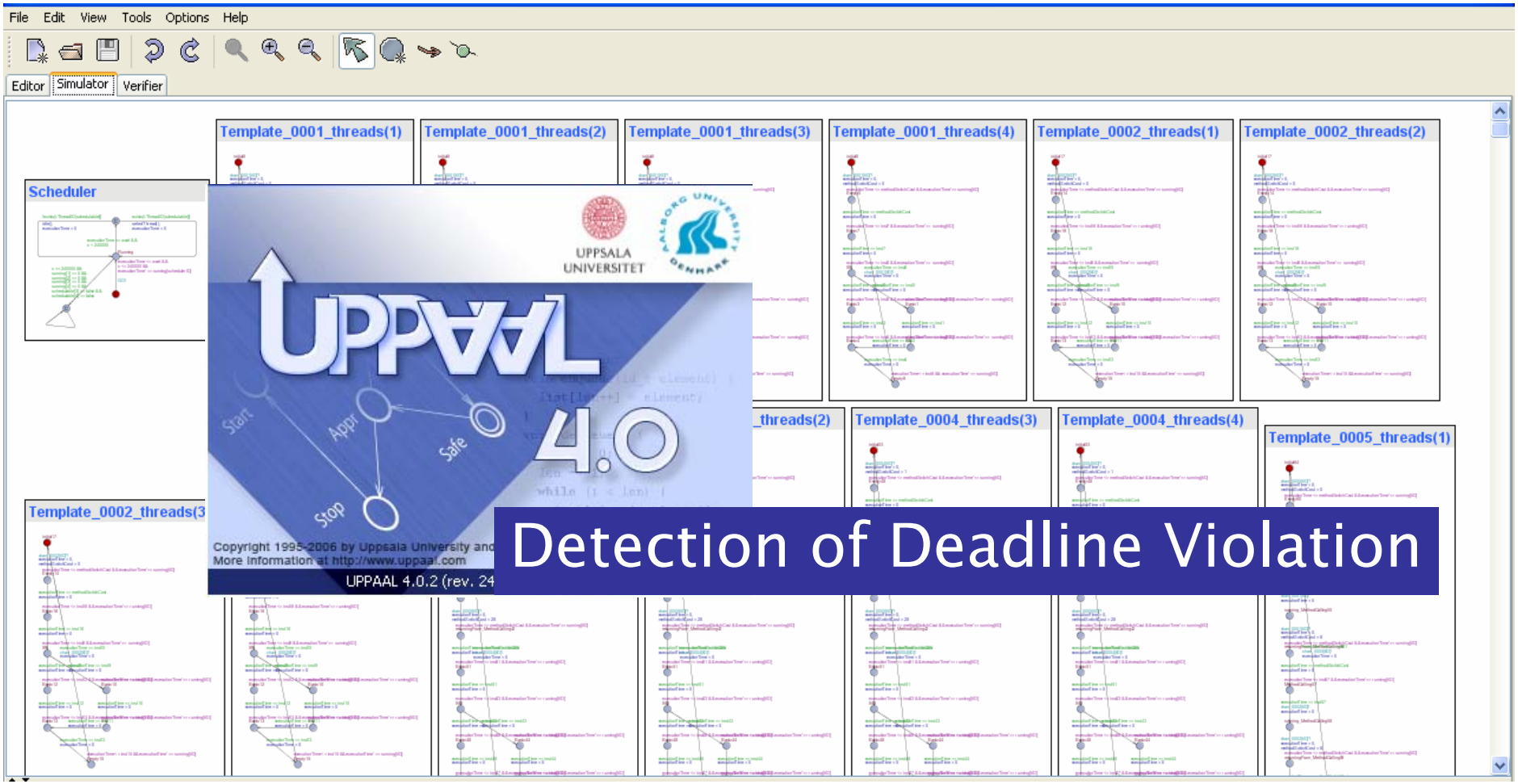
```
private void handleBrick() {
private void handleBrick() {
private void handleBrick() {
private void handleBrick() {
private void handleBrick() {
Sensors.synchronizedReadSensors();
int input = (Sensors.getBufferedSensor(0) + Sensors
                .getBufferedSensor(1)) >> 1;

if (awaitingBrick) {
        if (input > lastRead) {
                lastRead = input;
        } else if ((lastRead - input) >= TRESHOLD) {
                awaitingBrick = false;
                if (lastRead > BRICK_DETECTED) {
                        brickFound(lastRead);
                }
        }
```

METHODS

SARTS – to Timed Automata

Ingeniøren ELEKTRONIK-08

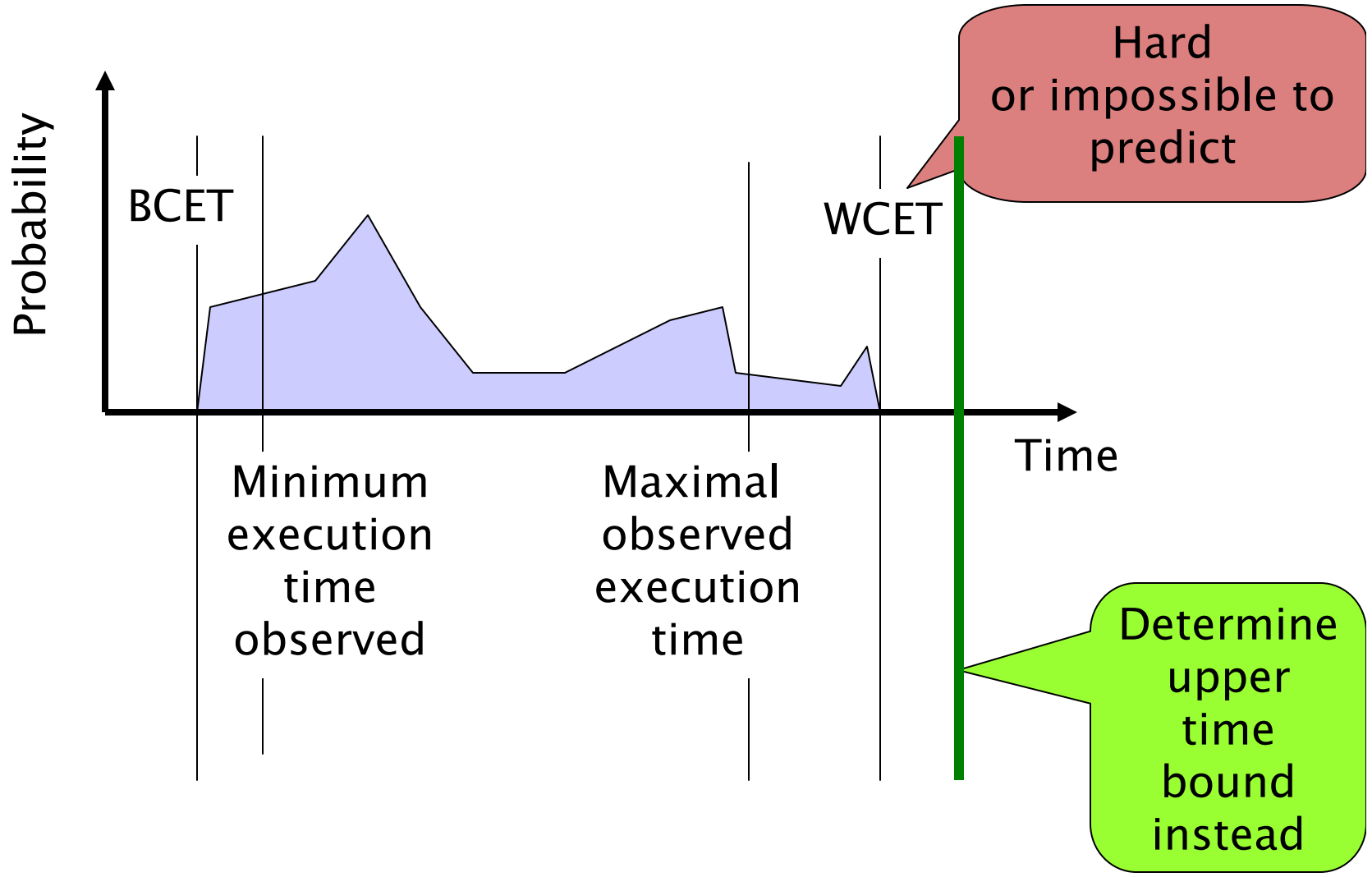


Detection of Deadline Violation

18 methods + 4 tasks = 76 components

WCET: Worst Case Execution Time

Ingeniøren ELEKTRONIK-08

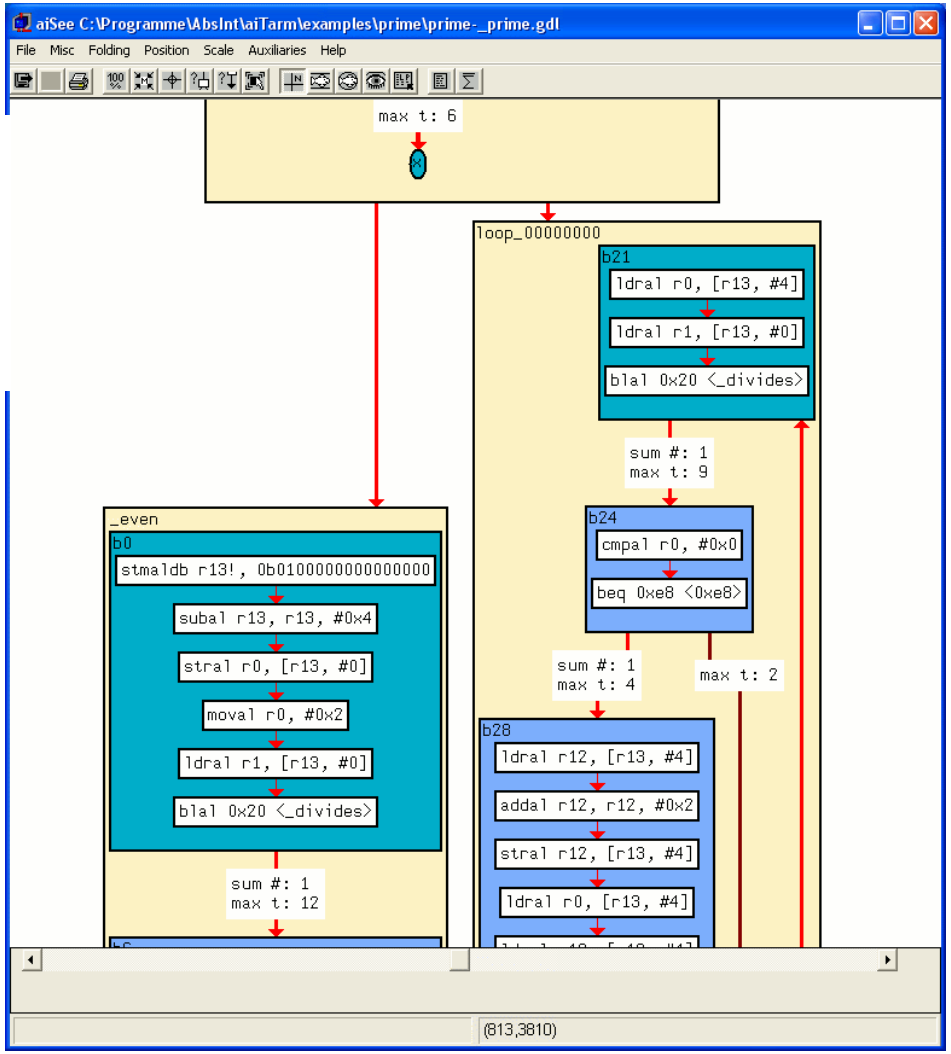


AbsInt – WCET state-of-the-art

Ingeniøren ELEKTRONIK-08

aiT for ARM7 TDMI
max t describes the maximum execution time of the basic block

AbsInt Angewandte Informatik

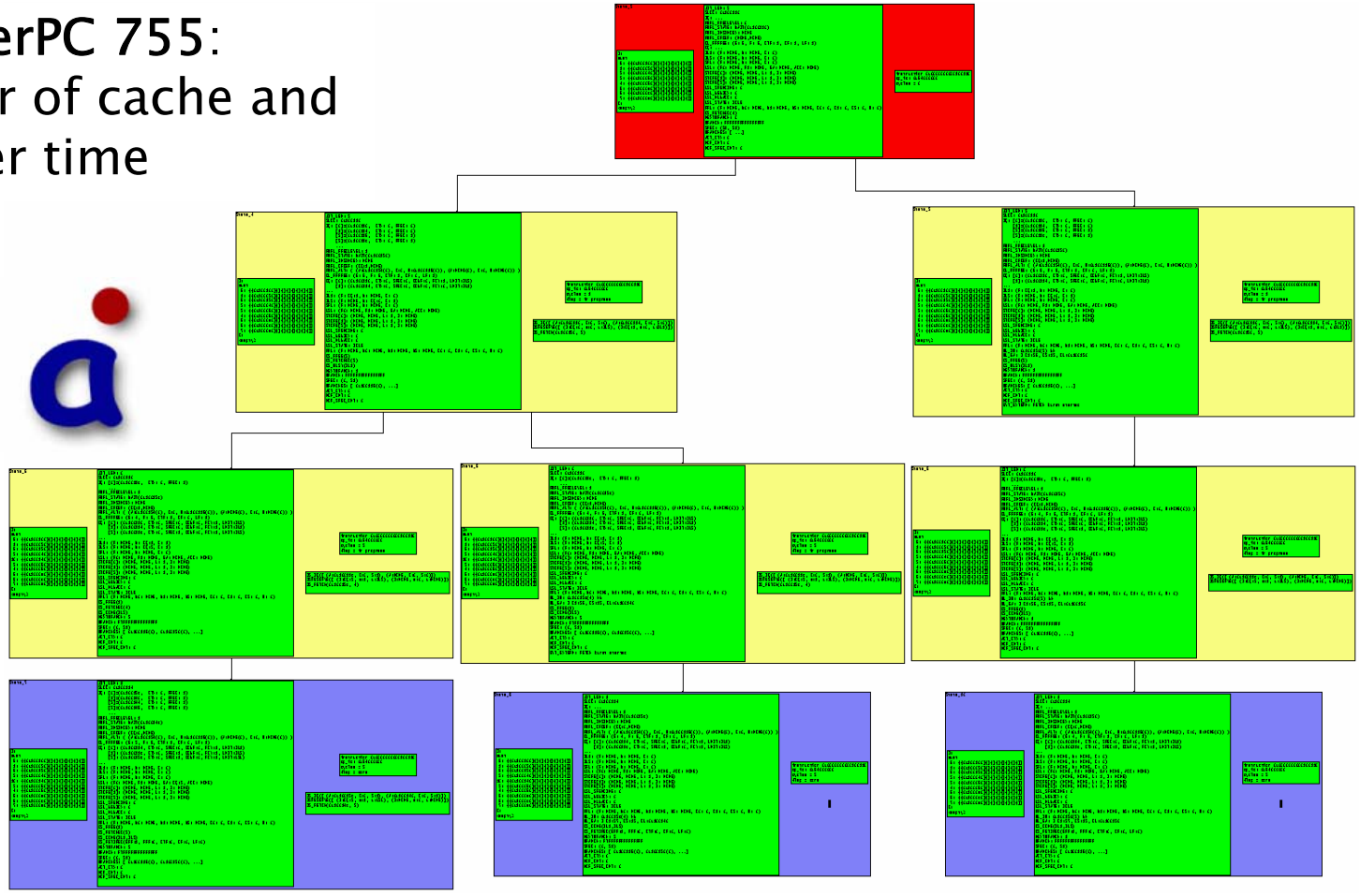


AbsInt – WCET state-of-the-art

Ingeniøren ELEKTRONIK-08

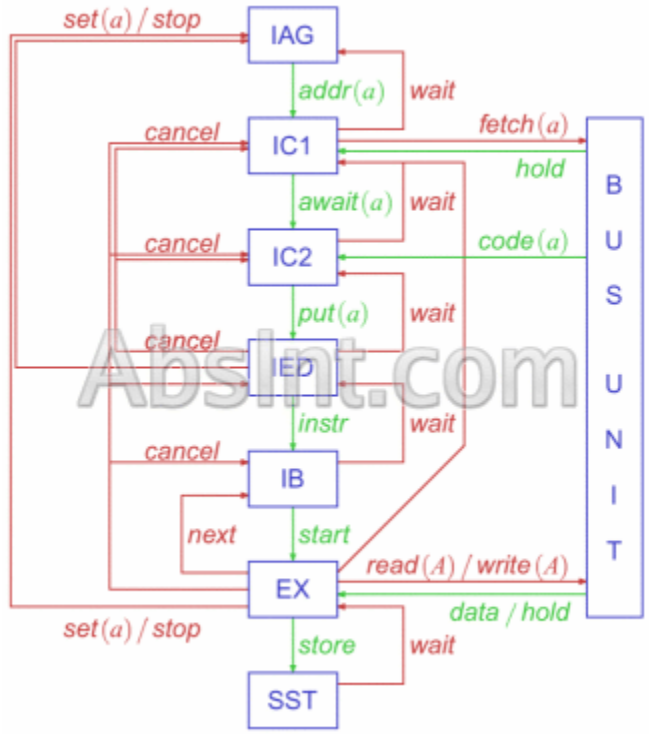
aiT for PowerPC 755:
the behavior of cache and pipeline over time

AbsInt
Angewandte Informatik



aiT for ColdFire 5307:
Map of the formal pipeline model used for timing validation.

AbsInt
Angewandte Informatik



AbsInt – WCET state-of-the-art

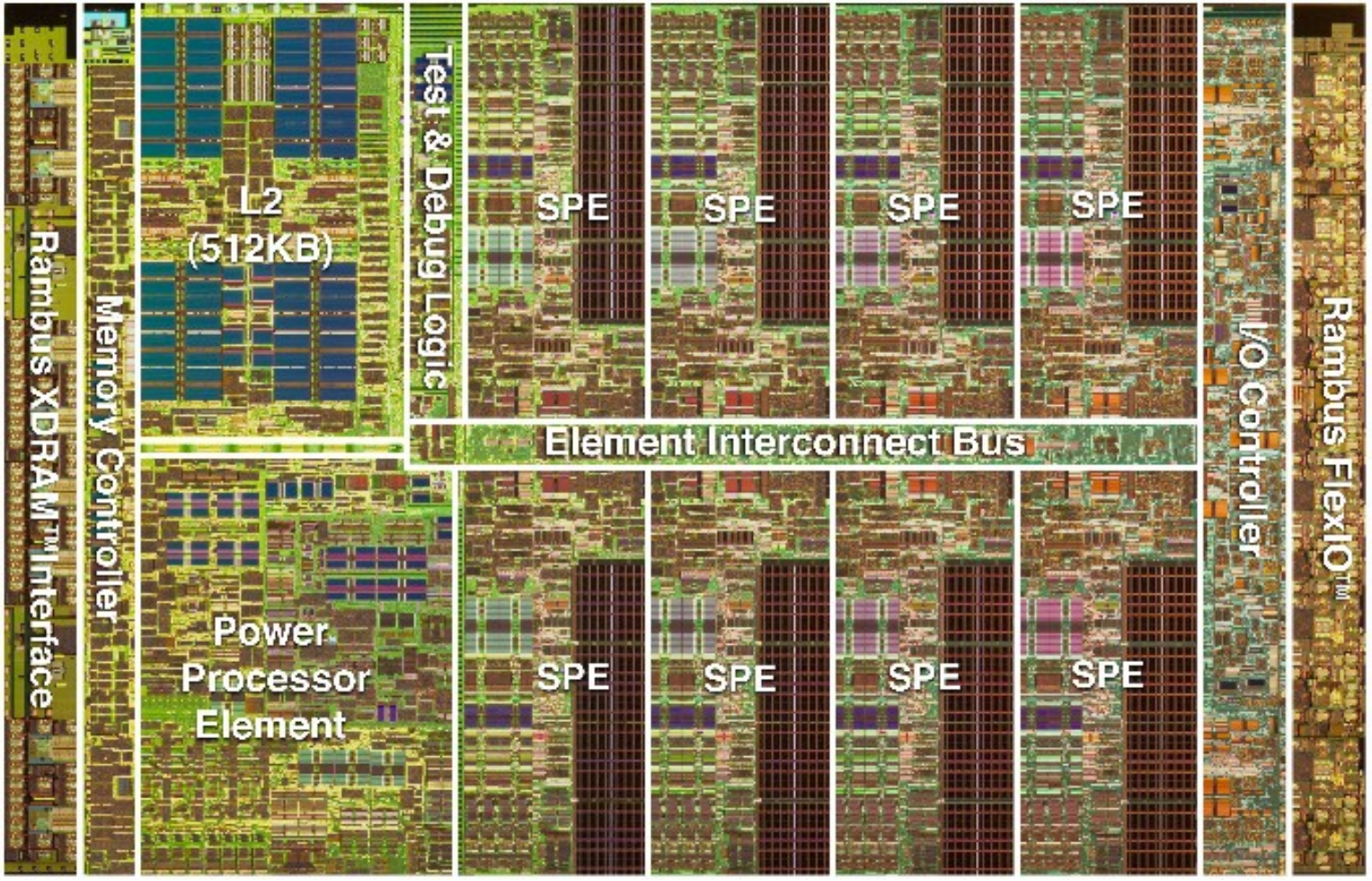
Ingeniøren ELEKTRONIK-08

Experiment	Target Processor	Average WCET overestimation	
			her Methods
Review by Airbus	MPC7	<25%	"useless"
Review on Vo code		16%	212%
Tests with ASCET	ST10	3%	–
aiT vs ARM			–
WCET Tool Challenge	C16x, ARM7, MPC565	7–8%	81%

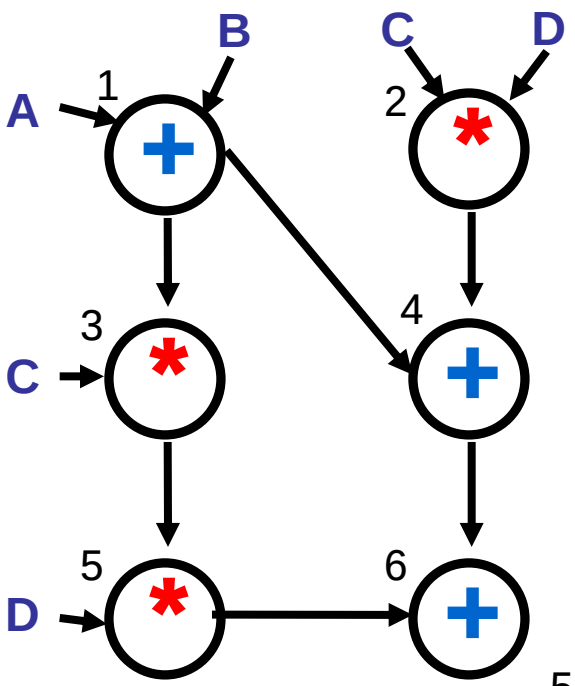
STATIC ANALYSIS

INTEGER LINEAR PROGRAMMING

The CELL processor



Optimal Scheduling – Time



Compute :

(D * (C * (A + B)) + ((A + B) + (C * D))

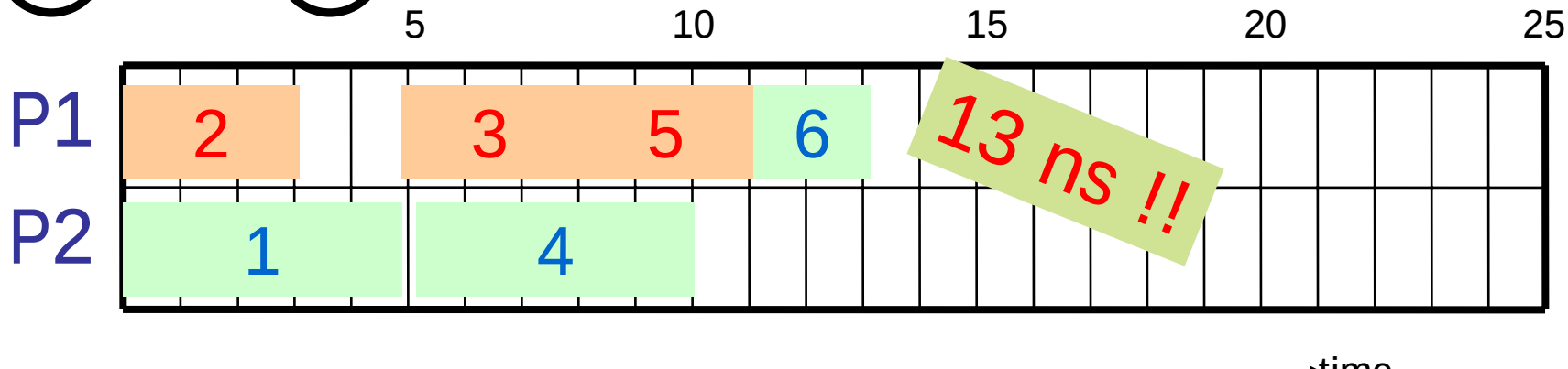
using 2 processors

P1 (fast)

+	2ns
*	3ns

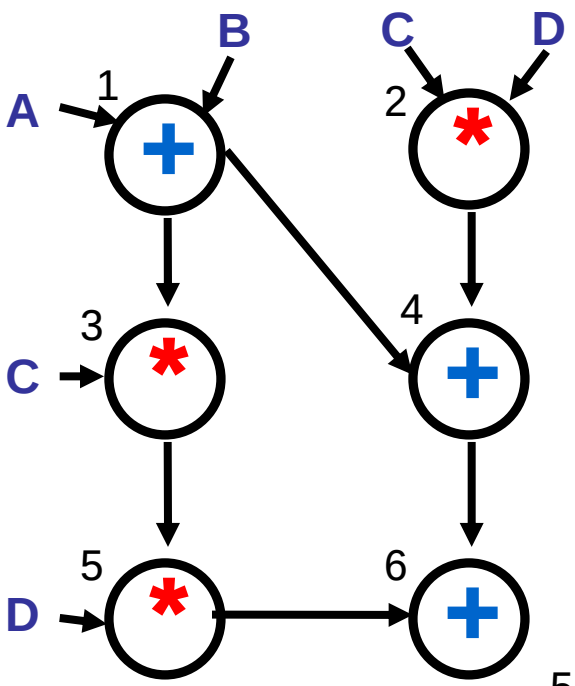
P2 (slow)

+	5ns
*	7ns



Optimal Scheduling – Time

Ingeniøren ELEKTRONIK-08



Compute :

(D * (C * (A + B)) + ((A + B) + (C * D))

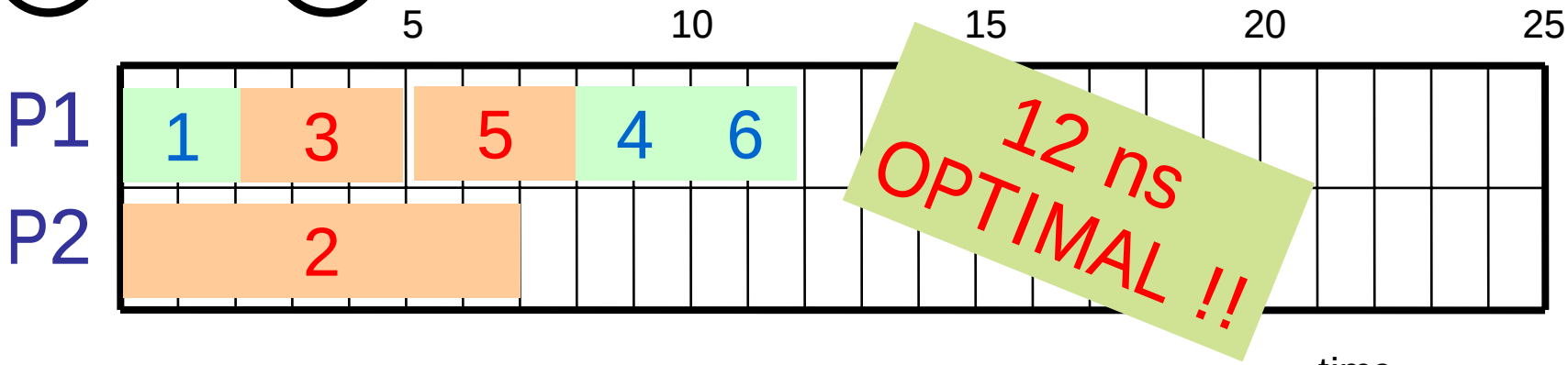
using 2 processors

P1 (fast)

+	2ns
*	3ns

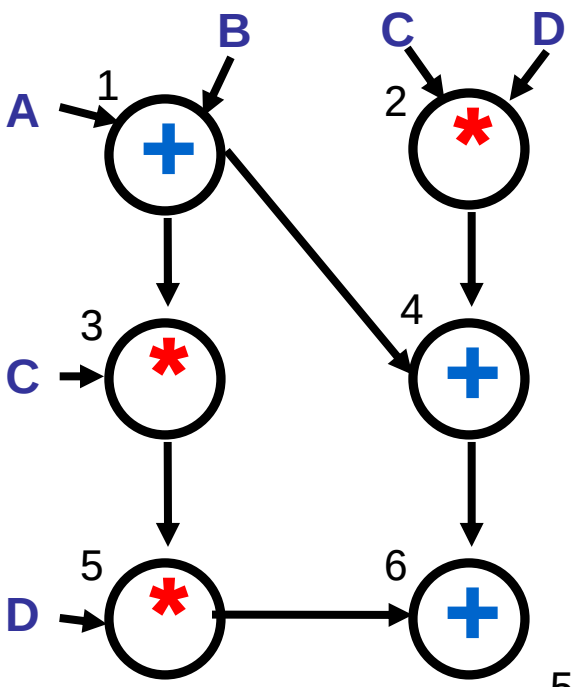
P2 (slow)

+	5ns
*	7ns



Optimal Scheduling – Power

Ingeniøren ELEKTRONIK-08



Compute :

(D * (C * (A + B)) + ((A + B) + (C * D))

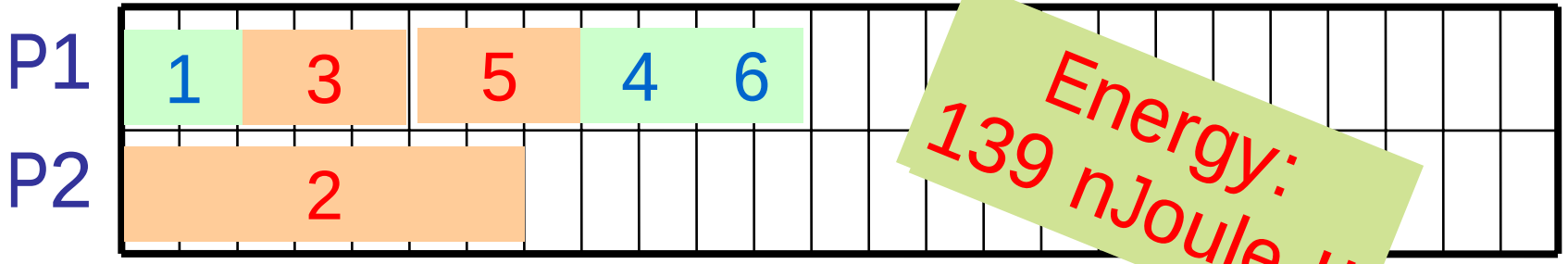
using 2 processors

P1 (fast) **P2** (slow)

+	2ns
*	3ns
Idle	1W
In use	9W

+	5ns
*	7ns
Idle	2W
In use	3W

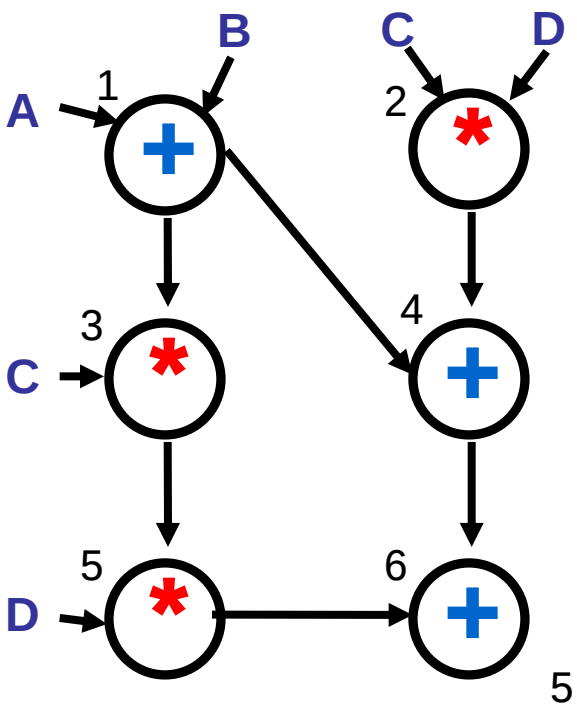
ENERGY:



Energy: 139 nJoule !!

Optimal Scheduling – Power

Ingeniøren ELEKTRONIK-08



Compute :

(D * (C * (A + B)) + ((A + B) + (C * D))

using 2 processors

P1 (fast) **P2** (slow)

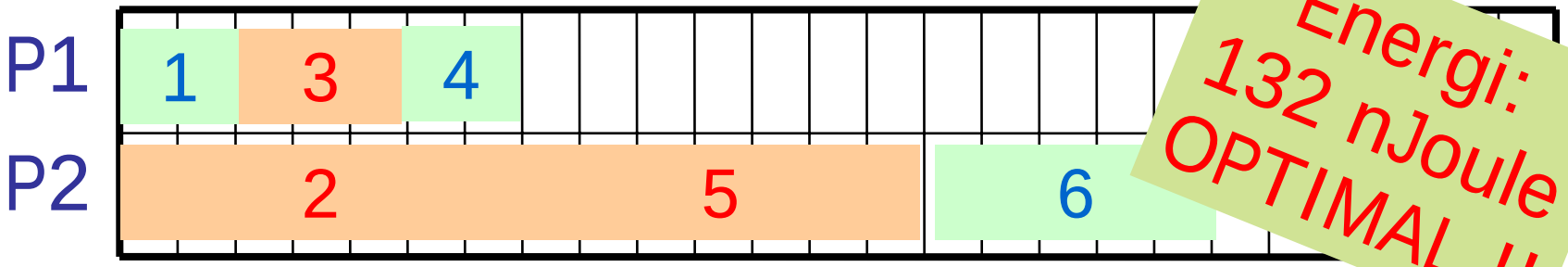
+	2ns
*	3ns
Idle	1W
In use	9W

+	5ns
*	7ns
Idle	2W
In use	3W

ENERGY:

10

5

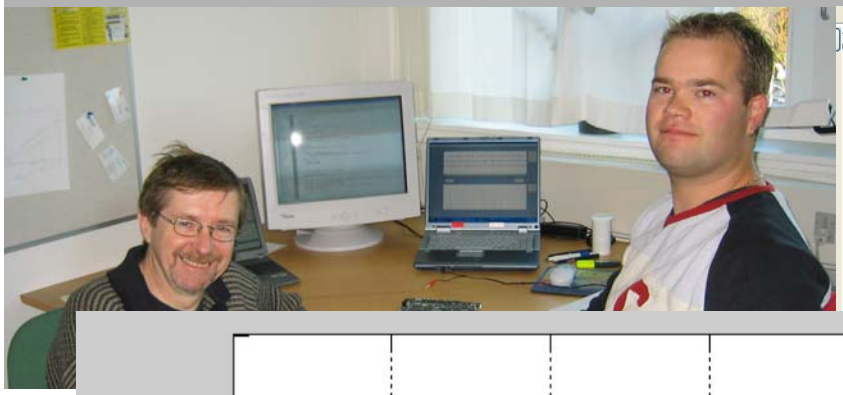


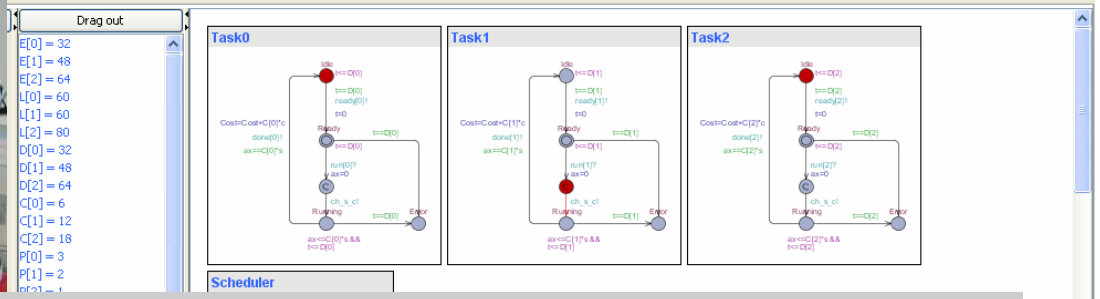
Energi:
132 nJoule
OPTIMAL !!

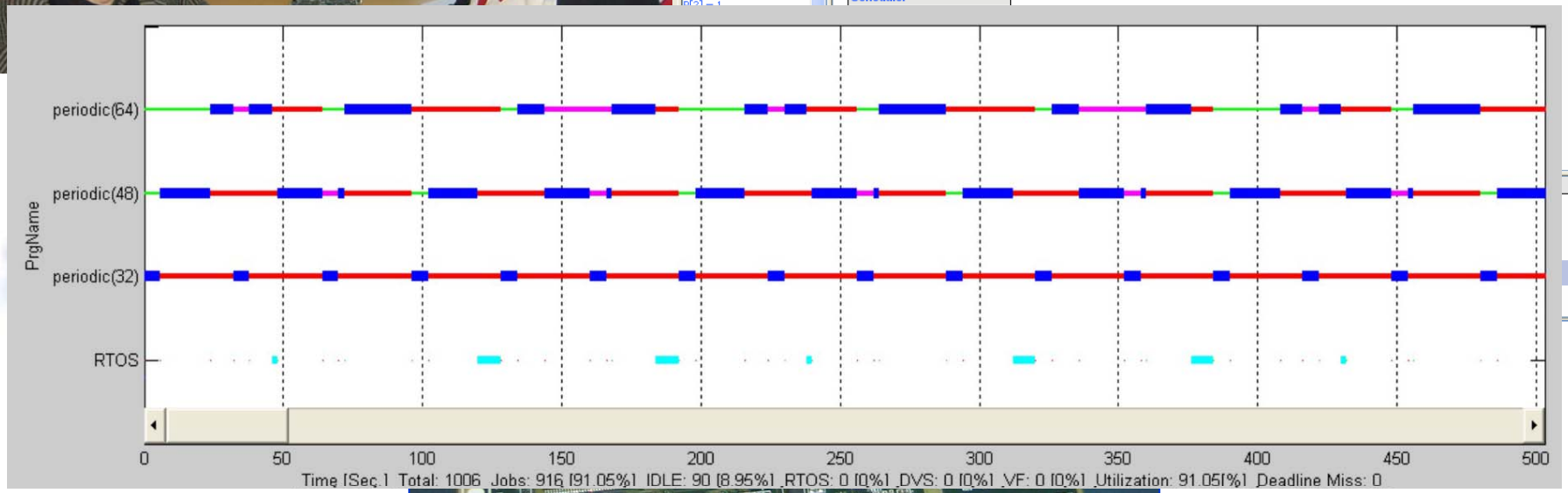
Power Management

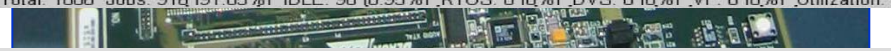
Ingeniøren ELEKTRONIK-08

Dynamic Voltage Scaling









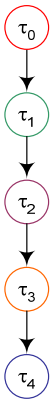
Dynamically lower voltage supply (frequency) to utilize free CPU time [A. Skou & A. Brødløs]

Handling Realistic Applications?

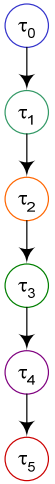
Ingeniøren ELEKTRONIK-08

Jan Madsen / DTU

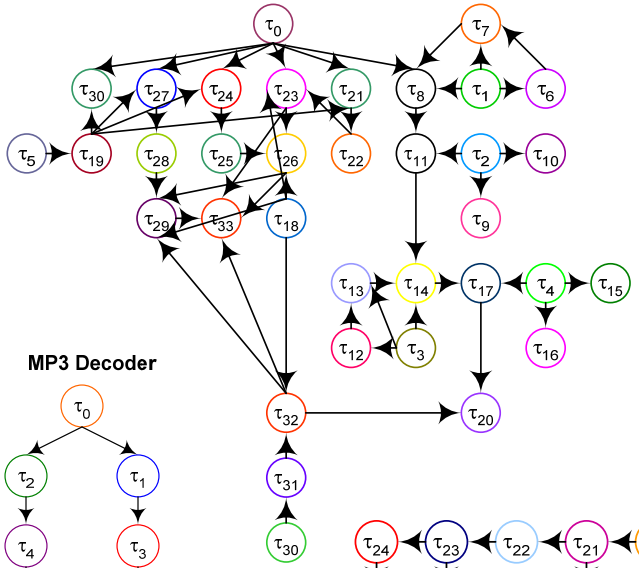
JPEG Encoder



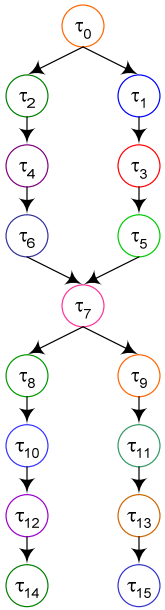
JPEG Decoder



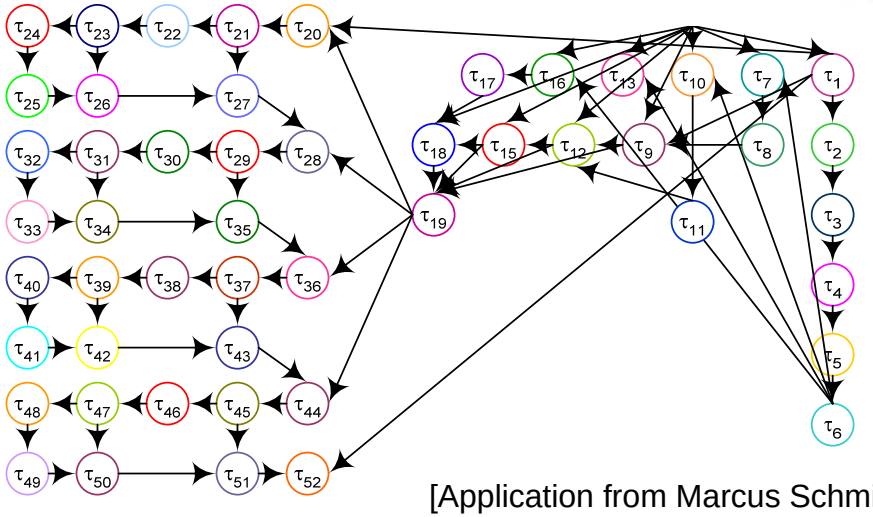
GSM Decoder



MP3 Decoder



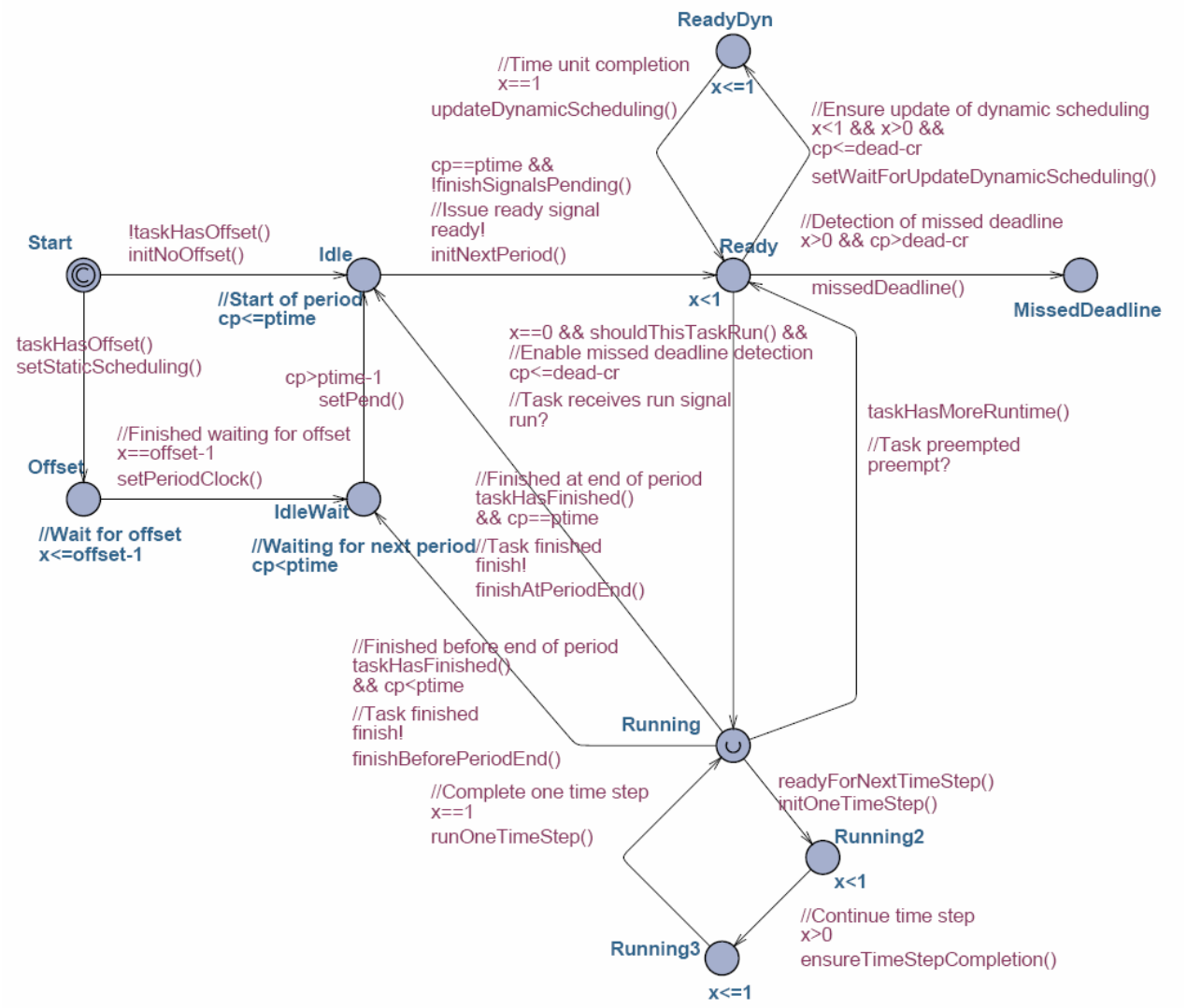
GSM Encoder



Smart phone:

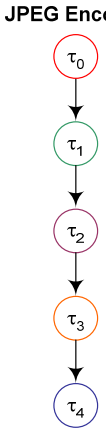
[Application from Marcus Schmitz, TU Linkoping]

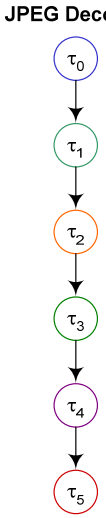
Timed Automata for a Task

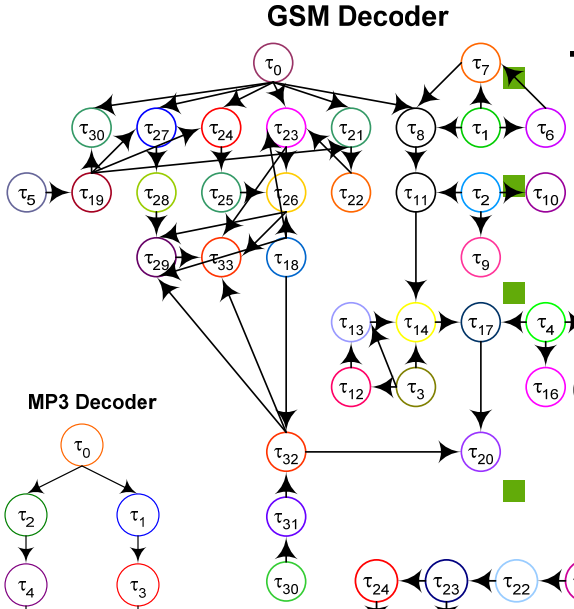


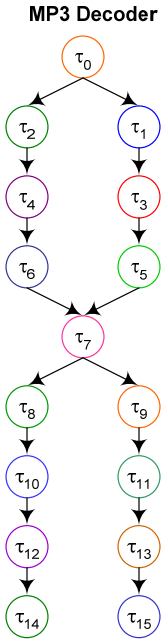
Smart Phone

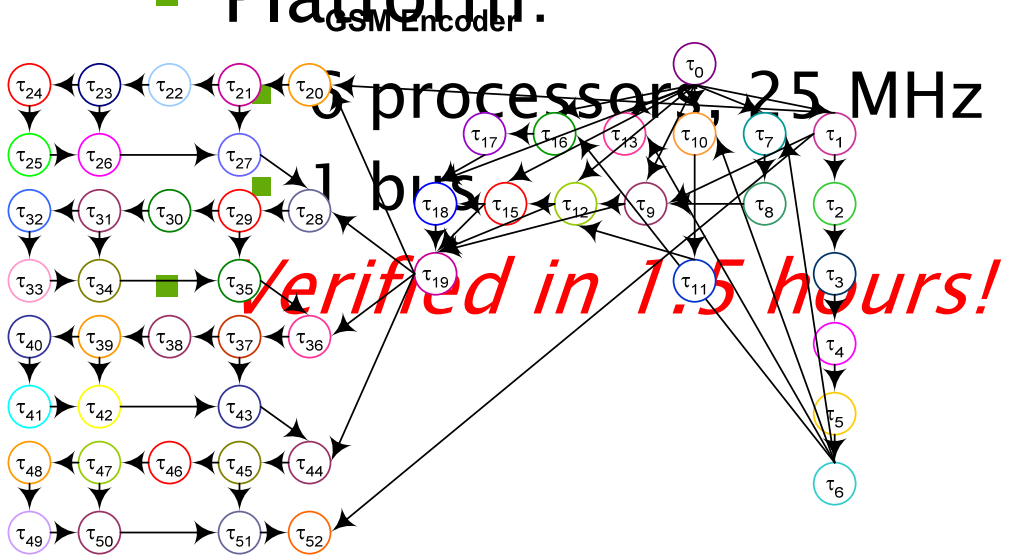
Ingeniøren ELEKTRONIK-08











- Tasks: 114
- Deadlines: [0.02: 0.5] sec
- Execution: [52 : 266.687] cycles
- Platform:
  - 5 processors, 25 MHz
  - 1 bus

Verified in 1.5 hours!

Tools for Performance Analysis

Ingeniøren ELEKTRONIK-08

Simulation

- CoFluent Studio
- Mentor Graphics Catapult
- SystemC
- ARTS
- Matlab/Simulink
- TrueTime
- Ptolemy

Analysis

- Esterel Studio
- AbsInt
- SymTA
- UPPAAL
- Design Trotter
- TIMES

DaNES – Højteknologisk Platform

Højteknologifonden

DaNES

Danish Network for Intelligent Embedded Systems

About DaNES Research Events Partners Positions Links Contact Extranet

You are here: Home

[Wednesday, 20th February. ARTISTDesign Kick-off]

DaNES is heavily involved in ARTIST Design with CISS coordinating the activities on Modelling and Validation and DTU coordinating the activities on Hardware Platform and MPSoC Design.
The kick-off meeting of the new European Network of Excellence ARTIST Design was held in Paris on January 29 and 30, 2008.
Read more

[Wednesday, 20th February. Jan Madsen on ARTEMIS board]

Professor Jan Madsen,

Danish Network for Intelligent Embedded Systems

DaNES is a consortium - read about the partners here.

You are now logged in as **Kim Guldstrand Larsen**.
Logout

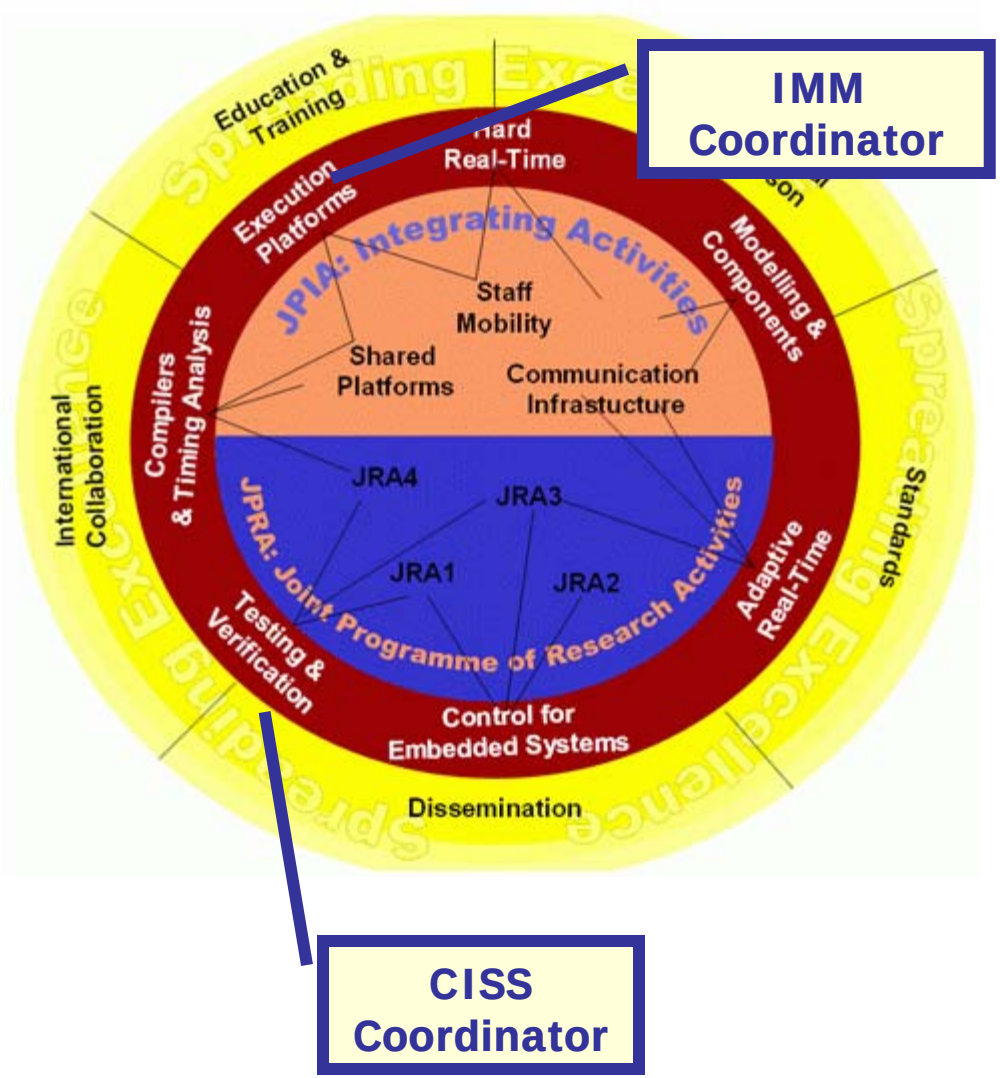
Novo Nordisk teams up with CISS: UppAAL modelling reveals protocol deficiencies

Pursuing a DaNES activity, a communication protocol for a medical device was modelled and analyzed using UppAAL, revealing protocol deficiencies. Pending specification

parameter optimization.

www.danes.aau.dk

Network of Excellence



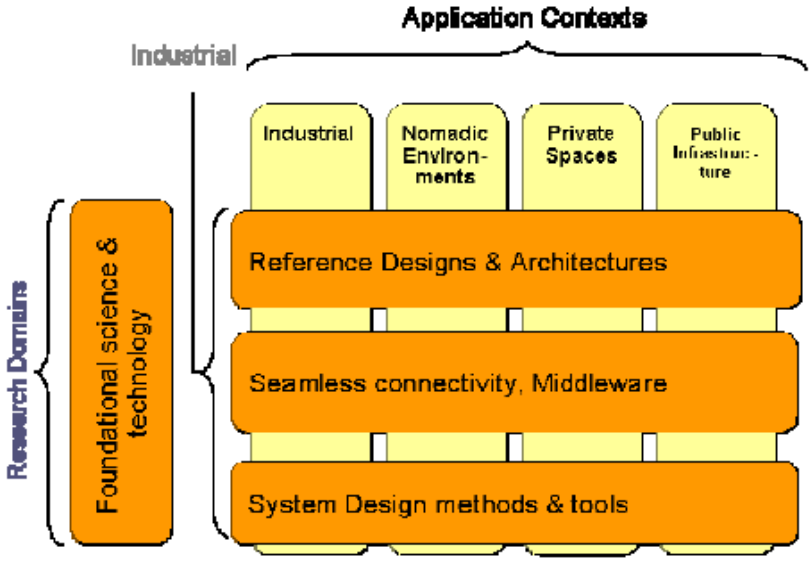
32 academiske partners

Affiliated companies:

- ABB Automation
- Airbus
- Daimler Chrysler AG
- Electricite de France
- Ericsson Mobile Platforms
- ESA
- Honeywell
- Israel Aircraft
- Nokia Denmark
- Siemens MP
- STMicroelectronics
- Sun Microsystems
- Thales
- Volkswagen AG
- Volvo Car

ARTEMIS

Ingeniøren ELEKTRONIK-08



SP1: Metoder og processer inden for sikkerhedskritiske indlejrede systemer.

SP2: Personcentreret helbredshåndtering.

SP3: Smarte omgivelser og skalerbare digitale services.

SP4: Effektiv produktion og logistik.

SP5: Programomgivelser for indlejrede systemer.

SP6: Sikkerhed (security), privathed og pålidelighed.

SP7: Indlejret teknologi for bæredygtigt byliv.

SP8: Menneskecentreret design af indlejrede systemer.

D-ARTEMIS

Ingeniøren ELEKTRONIK-08

ITEK

Alexandra Instituttet A/S

DaNES
Danish Network for Intelligent Embedded Systems

DTU

Center for Indlejrede Software Systemer

University of Southern Denmark
mci mads clausen institute

Solidum petit in profundis · Universitas Arhusiensis

- Deltagelse i ARTEMIS governing board
- Påvirkning af strategisk forskningsplan gennem ARTEMISIA og ARTIST
- Matchmaking på nationalt plan
- Matchmaking på internationalt plan
- Synliggørelse af calls.
- Koordinering af ansøgninger.

Thank you!

kgl@ciss.dk
www.ciss.dk